

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Appl. No.	:	10/710,699	Confirmation No. 4698
Applicant	:	Somasekar Jayaraman	Customer No. 23494
Filed	:	07/29/2004	
TC/A.U.	:	2825	
Examiner	:	Parihar, Suchin	
Docket No.	:	TI-37107	
Title	:	ACCURATE TIMING ANALYSIS OF INTEGRATED CIRCUITS WHEN COMBINATORIAL LOGIC OFFERS A LOAD	

**RESPONSE TO OFFICAL ACTION UNDER 35 C.F.R. § 1.111**

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action mailed February 10, 2006, Applicant respectfully submits the following amendments and remarks in connection with the above identified application.

**Amendments to the Specification** begin on page 2 of this paper.

**Amendments to the Claims** begin on page 3 of this paper.

**Remarks** begin on page 6 of this paper.